CLAIMS

What is claimed is:

1. A process comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures.

2. The process according to claim 1, further including:

implanting a self-aligned collector tap in the self-aligned recess.

3. The process according to claim 1, wherein forming a self-aligned recess further includes:

patterning a mask that exposes a portion of the first isolation structure, a portion of the emitter stack, and a portion of the substrate located between the first isolation structure and the emitter stack; and

etching the self-aligned recess with an etch recipe that is more selective to the first isolation structure and the emitter stack than to the substrate.

4. The process according to claim 1, wherein forming a self-aligned recess further includes:

patterning a mask that exposes a portion of the first isolation structure, a portion of the emitter stack, and a portion of the substrate located between the first isolation structure and the emitter stack; and

anisotropically etching the self-aligned recess with an etch recipe that is more selective to the first isolation structure and the emitter stack than to the substrate.

5. The process according to claim 1, wherein implanting a self-aligned collector tap in the self-aligned recess includes:

patterning a mask that exposes at least a portion of the first isolation structure and the emitter stack; and

implanting a dopant into the substrate that is exposed by the self-aligned recess.

6. The process according to claim 1, wherein implanting a self-aligned collector tap in the self-aligned recess includes:

patterning a mask that exposes at least a portion of the first isolation structure and the emitter stack; and

implanting a dopant into the substrate that is exposed by the recess, wherein implanting results in a P-- collector tap, a P- collector tap, a P collector tap, a P+ collector tap, a P++ collector tap, an N-- collector tap, an N- collector tap, an N collector tap, an N+ collector tap, and an N++ collector tap.

7. The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon.

8. The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer;

patterning the polysilicon film into emitter polysilicon; and

forming a spacer on the emitter stack.

9. The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, implanting a collector structure;

in the substrate, forming an epitaxial layer;

forming a polysilicon film over the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon, wherein the emitter polysilicon is disposed above the collector structure.

10. The process according to claim 1, wherein forming an emitter stack includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer;

patterning the polysilicon film into emitter polysilicon, wherein patterning the polysilicon film into emitter polysilicon further includes:

patterning a hard mask above the polysilicon film.

11. The process according to claim 1, wherein forming an emitter stack includes:

in the substrate, forming an epitaxial layer;

forming a dielectric layer above the epitaxial layer;

forming an emitter cut in the dielectric layer;

forming a polysilicon film above the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon.

12. The process according to claim 1, further including:

in the substrate, forming a buried layer.

13. A bipolar junction transistor comprising:

in a substrate, a first isolation structure spaced apart from a second isolation structure;

an emitter stack disposed above the substrate and between the first isolation structure and the second isolation structure;

a recess disposed adjacent and between the emitter stack and the first isolation structure, wherein the recess exposes a collector tap.

14. The bipolar junction transistor according to claim 13, further including:

a spacer disposed on the emitter stack, wherein the spacer extends on one side thereof into the recess between the emitter stack and the first isolation structure.

15. The bipolar junction transistor according to claim 13, further including:

a spacer disposed on the emitter stack, wherein the spacer extends on one side thereof into the recess between the emitter stack and the first isolation structure, and wherein the spacer is selected from an oxide, a nitride, an oxide first layer and a nitride second layer, a nitride first layer and an oxide second layer, an oxide first layer and an oxide second layer, and a nitride first layer and a nitride second layer.

16. The bipolar junction transistor according to claim 13, further including:

a spacer disposed on the emitter stack, wherein the spacer extends on one side thereof into the recess between the emitter stack and the first isolation structure, and wherein the spacer is further disposed on the first isolation structure and extends into the recess.

17. The bipolar junction transistor according to claim 13, further including:

a buried layer disposed in the substrate between the first isolation structure and the second isolation structure.

18. The bipolar junction transistor according to claim 13, further including:

in the substrate, an epitaxial base layer disposed below the emitter stack;

a collector structure disposed in the substrate below the emitter stack; and

an intrinsic base structure disposed between the emitter stack and the collector structure.

19. The bipolar junction transistor according to claim 13, further including:

in the substrate, an epitaxial base layer disposed below the emitter stack;

a collector structure disposed in the substrate below the emitter stack;

a dielectric layer disposed above the substrate and below the emitter stack, wherein the dielectric layer includes an emitter cut disposed above the collector structure; and

an intrinsic base structure disposed between the emitter cut and the collector structure.

20. The bipolar junction transistor according to claim 13, further including:

in the substrate, a collector tap disposed in the recess, wherein the collector tap is selected from a P-- collector tap, a P- collector tap, a P collector tap, a P+ collector tap, a P++ collector tap, an N-- collector tap, an

N- collector tap, an N collector tap, an N+ collector tap, and an N++ collector tap.

21. The bipolar junction transistor according to claim 13, wherein the substrate includes a bipolar-complementary metal oxide semiconductor (BiCMOS) structure.

22. The bipolar junction transistor according to claim 13, wherein the BJT is selected from a monojunction BJT device and a heterojunction BJT device.

23. A bipolar junction transistor (BJT) layout comprising:

an epitaxial base layer perimeter;

an emitter stack perimeter disposed above the base layer perimeter; and

a collector tap perimeter, wherein the emitter stack perimeter and the collector tap perimeter share a co-linear first boundary.

24. The BJT layout according to claim 23, wherein the emitter stack perimeter and the epitaxial base layer perimeter intersect.

25. The BJT layout according to claim 23, wherein the collector tap perimeter shares a co-linear second boundary and a co-linear third boundary with the epitaxial base layer perimeter.

26. The BJT layout according to claim 23, further including:

a base tap perimeter, wherein the base tap perimeter is enclosed by the epitaxial base layer perimeter.